REMARKS

Favorable reconsideration of this application, in light of the following remarks, is respectfully requested.

Claims 1-21 are pending in this application.

Specification

The title of the present application has been amended to "THREAD SELECTION FOR FETCHING INSTRUCTIONS FOR PIPELINE MULTI-THREADED PROCESSOR" per the Examiner's suggestion. Withdraw of the Examiner's objection is requested.

Rejections under 35 U.S.C. §102

Claims 1-21 stand rejected under 35 U.S.C. §102(b) as being anticipated by Emer et al. (U.S. Patent No. 6,073,159). The Applicants respectfully traverse this rejection for the reasons detailed below.

The Examiner alleges that Emer et al. discloses all the features of independent claim 1. Without acquiescing to the Examiner's other rejection reasons, Applicants note that the Examiner alleges that column 6, lines 22-45, teaches the feature "the fetch unit receiving information from at least one other stage of the processing pipeline[.] (Emphasis added.) The Examiner specifically alleges that "The fetch unit receives thread attribute information and determines an estimated processing time of each thread[,]" discloses the feature of claim 1. The Examiner's quoted passage fails to teach or suggest that the fetch unit receives any information from any other stage of the processing pipeline.

As can be seen in FIG. 2 of Emer et al., none of the stages in the processing pipeline transmits information back to the fetch unit. Emer et al. fails to teach or suggest all the features of claim 1; therefore, for at least the reason given above, claim 1 is patentable over the cited reference. Similarly recited independent claim 13 is also patentable for the same reasons given above with respect to the patentability of claim 1.

Claims 2-12 and 14-21, dependent on independent claims 1 and 24, respectively, are patentable for the reasons stated above with respect to claims 1 and 21 as well as for their own merits.

Rejections under 35 U.S.C. §102

Claims 1 and 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Borkenhagen et al. (U.S. Patent No. 6,073,159). The Applicants respectfully traverse this rejection for the reasons detailed below.

The Examiner alleges that Borkenhagen et al. discloses all the features of claims 1 and 13. The Examiner specifically alleges that Borkenhagen et al. discloses the feature "the fetch unit receiving information from at least one other stage of the processing pipeline and determining a processing time of the processing pipeline occupied by each thread based on the received information." For support, the Examiner cites column 7, lines 29-33, and the Examiner further alleges that "The thread switch time-out register is part of the instruction unit." Applicants disagree.

Without acquiescing to the Examiner's other reasons for rejection, first, column 7, lines 29-33 has nothing to do with thread switch logic, an instruction unit, or a thread switch time-out register, but rather is a general statement regarding the conventional processor. Second, a thread

switch time-out register 430 is part of thread switch logic 400, and not part of an instruction unit 220, as alleged by the Examiner. Please see FIG. 4A. Further, column 15, lines 1-43, discloses that a thread switch time-out value is loaded by hardware into a decremented register.

Even assuming thread switch time-out value is equivalent to information received by the fetch unit as recited in claims 1 and 13, nowhere in Borkenhagen et al. does it disclose that the thread switch time-out value is received by the instruction unit, nor does it disclose that the instruction unit use the information to determine a processing time of the pipeline occupied by each thread. Accordingly, Borkenhagen et al. fails to disclose all the features of claim 1 and similarly recited claim 13. For at least the reasons given above, claims 1 and 13 are patentable over the Examiner's cited reference.

CONCLUSION

In view of the above remarks and amendments, the Applicants respectfully submit that each of the pending objections and rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any

additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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